AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Original) An electrostatic discharge protection device comprising:

a first bipolar transistor and a second bipolar transistor coupled in series, and

an emitter of the first bipolar transistor being coupled to a protected node and an emitter of the second bipolar transistor being coupled to a grounded node, the first bipolar transistor and the second bipolar transistor having a common collector.

2. (Original) The electrostatic discharge protection device of claim 1, the first bipolar transistor and the second bipolar transistor being npn transistors.

3. (Original) The electrostatic discharge protection device of claim 1 further comprising a clamp electrically coupled between the protected node and a base of the second bipolar transistor.

4. (Original) The electrostatic discharge protection device of claim 3, the clamp comprising a two-terminal circuit.

5. (Original)The electrostatic discharge protection device of claim 4, the two-terminal circuit being configured to breakdown before the first and second bipolar transistor break down to reduce the overall trigger voltage of electrostatic discharge protection device.

6. (Currently Amended)The electrostatic discharge protection device of claim 4, the two-terminal circuit comprising at least one of ~~an n-moat-p-well diode,~~ a bipolar npn transistor, a bipolar pnp transistor, an NMOS transistor, and a PMOS transistor.

7. (Original) The electrostatic discharge protection device of claim 2, the common collector being formed by a first n-type region.

8. (Original)The electrostatic discharge protection device of claim 2, the first n-type region being coupled to a first p-type region and a second p-type region, the first p-type region forming a base of the first bipolar transistor, the second p-type region forming a base of the second bipolar transistor.

9. (Original) The electrostatic discharge protection device of claim 8, comprising an n-type doped isolation region that substantially surrounds and separates the first p-type region and the second p-type region.

10. (Original)The electrostatic discharge protection device of claim 9, comprising a second n-type region and a third n-type region, the second n-type region being formed within the first p-type region and separated from the first n-type region, the third n-type region being formed within the second p-type region and separated from the first n-type, the second n-type region forming the emitter of the first bipolar transistor and the third n-type region forming the emitter of the second bipolar transistor.

11. (Original) An electrostatic discharge protection device comprising:

a p-type semiconductor substrate;

an n-type buried layer provided in the p-type semiconductor substrate;

a first p-type region and a second p-type region overlying the n-type buried layer, the first p-type region and the second p-type region being separated from one another;

a first n^+ type region provided in the first p-type region;

a second n^+ type region provided in the second p-type region; and

the first n^+ type region, the first p-type region, and the n-type buried layer forming a first bipolar npn transistor, the second n^+ type region, the second p-type region, and n-type buried layer forming a second bipolar npn transistor, the first bipolar npn transistor and the second bipolar npn transistor including a common collector.

12. (Original) The electrostatic discharge protection device of claim 11, the first bipolar npn transistor and the second bipolar npn transistor being coupled in series.

13. (Original) The electrostatic discharge device of claim 12, further comprising an n-well isolation region that separates the first p-type region and the second p-type region.

14. (Original)The electrostatic discharge device of claim 11, the first n^+ type region functioning as an emitter of the first bipolar npn transistor, and the second n^+ type region functioning as an emitter of the second bipolar npn transistor.

15. (Original)The electrostatic discharge device of claim 14, the first p-type region functioning as a base region of the first bipolar npn transistor, and the second p-type region functioning as a base region of the second bipolar npn transistor.

16. (Original) The electrostatic discharge device of claim 15, the n-type buried layer functioning as a common collector for both the first bipolar npn transistor and the second bipolar npn transistor.

17. (Original)The electrostatic discharge protection device of claim 16, further comprising a two-terminal circuit electrically coupled between a protected node and the base of the second bipolar transistor, the two terminal circuit configured to break down before the first and second bipolar transistor break down to reduce the trigger voltage of electrostatic discharge protection device.

18. (Currently Amended) A method for fabrication of an ESD protection device, the method comprising:

providing an n-type buried layer in a p-type semiconductor substrate;

~~forming a first p-type region and a second p-type region overlying the n-type buried layer;~~

forming a first p-type region and a second p-type region overlying the n-type buried layer, the first p-type region and the second p-type region being separated from one another;

forming a first n^+ type region in the first p-type region;

forming a second n^+ type region in the second p-type region; the first n^+ type region, the first p-type region, and the n-type buried layer defining a first bipolar npn transistor, the second n^+ type region, the second p-type region, and n-type buried layer defining a second bipolar npn transistor.

19. (Original)The method of claim 18, further comprising forming an n-well isolation region that separates the first p-type region and the second p-type region.

20. (Original)The method of claim 19, the first n+ type region functioning as an emitter of the first bipolar npn transistor, the second n+ type region functioning as an emitter of the second bipolar npn transistor, the first p-type region functioning as a base region of the first bipolar npn transistor, the second p-type region functioning as a base region of the second bipolar npn transistor, and the n-type buried layer functioning as a collector for both the first bipolar npn transistor and the second bipolar npn transistor.